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CONTROL OF ELECTRONIC CIRCUIT DESIGNS FOR SPACE VEHICLES

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16. Abstract

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SUMMARY

A technical management procedure that is directed to the design of a complex electronic system for space environment applications is described. The procedure was developed by the NASA Lewis Research Center and applied to the Centaur launch vehicle program. Specific controls used include a complete hierarchy of specifications, design ground rules, derating document, preferred parts list, worst-case design procedure, computer circuit analysis programs, and design reviews. The use of these rigorous design controls resulted in an electronic system capable of meeting its performance and reliability goals with a minimum of difficulty.

INTRODUCTION

In the past, design procedures for space vehicle electronic systems have been somewhat informal, and the task of developing much of the design criteria was left to individual circuit designers. Also, it was not thought to be practical to design electronic circuitry so that the system would meet its performance specifications and have an adequate reliability margin for worst-case conditions of environment and part parameter tolerance. In the early days of the program, the Centaur project experienced many difficulties because of informal design procedures. No problems were encountered in flight, but the manufacturing and testing phases were hampered by marginal designs. For example, at certain conditions of temperature and parameter tolerance, undesired voltage oscillations occurred on the output of a power supply. To correct this condition, electronic components had to be carefully selected.

Today, the availability of high-speed digital computers and circuit analysis programs has eased the task of performing an accurate worst-case analysis of circuits. Teaming a formalized worst-case design procedure with computer circuit analysis programs such as ECAP (ref. 1) will result in a reliable electronic system meeting its performance specifications.

This report describes a formal technical management procedure that is applicable to the design of a complex electronic system to be used in the space environment. Specific controls that are used in this procedure include

(1) A complete hierarchy of specifications

(2) Design ground rules

(3) Derating document and preferred parts list

(4) Worst-case circuit design procedures

(5) Computer circuit analysis programs

(6) Design reviews

The advantages of using a formal technical management procedure are as follows:

(1) Specifications are very detailed and thoroughly documented from the system specification to the individual electronic part and circuit level.

(2) Electronic and electromechanical parts are selected from a limited list of high-reliability parts, and a formal procedure with NASA control is called out for use of non-standard parts.

(3) Worst-case design of circuits is done in a consistent manner.

(4) The use of periodic design reviews allows NASA to maintain control of the system design.

(5) The design of the electronic system is thoroughly documented for the purpose of NASA review and to aid in the solution of any problems that may arise in the future.

The Lewis Research Center Centaur Project Office developed the described technical management procedure in 1965 and applied it to the design of an inertial guidance subsystem for the Centaur launch vehicle. This subsystem has operated according to specifications in 11 successive space flights. Currently, this technical management procedure is being applied to the design of new electronic systems for the same launch vehicle.

DESIGN PROCEDURE - GENERAL DESCRIPTION

The general description of the design procedure is aided with the block diagram of figure 1, which illustrates the major phases and factors of the design and their relations to each other. A detailed description is given later starting in the next section.

The system specifications is, of course, the foundation of the design. It provides the basic information to formulate the functional specifications for each electronic module or subsystem. The preliminary mechanical and thermal design is accomplished immediately after the system specifications are known. The reason for this early design work is that the system specification calls out a model for the thermal environment, and a rough thermal analysis has to be performed so that realistic thermal requirements can be incorporated into functional specifications for the electronic modules. The system

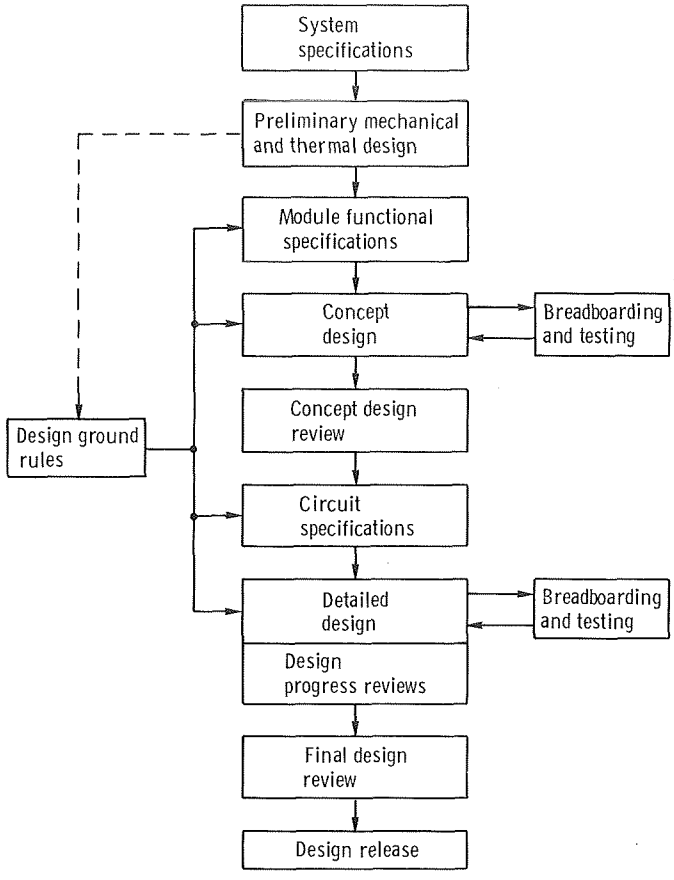

Figure 1. - Design procedure.

specification also calls out the shock and vibration environment; therefore, some preliminary mechanical stress calculations have to be performed in order to adequately specify the mechanical requirements for the electronic modules. Further mechanical and thermal design is done in the concept design stage to uncover any major problem before the system design has progressed very far.

The design ground rules provide inputs to the module functional specifications block and design blocks. The design ground rules designate ranges of design temperatures for the electronic modules based on the preliminary thermal analysis and call out maximum vibration amplification factors to use based on preliminary mechanical design. Further, these design ground rules require use of a common preferred parts list and derating document.

The concept design phase is devoted to studying alternate methods of design. Enough preliminary circuit analysis and breadboard testing, as well as mechanical and thermal design, are done to provide information for the concept design review. Preliminary de-

sign data are presented at the concept design review, and NASA approval is given for the detailed design of the selected method.

A complete set of circuit specifications is formulated at the start of the detailed design phase to serve as the basis for a worst-case design. Computer circuit analysis and thermal and mechanical stress programs are used in the detailed design phase. Progress design reviews are held periodically during this detailed design phase.

At the final design review, all design and testing documentation is reviewed to assure NASA that the design requirements have been met.

SPECIFICATIONS

Before any serious circuit design for the electronic system is attempted, a complete hierarchy of specifications needs to be generated. The requirements range from a top specification for the functional, physical, and environmental characteristics of the system to the detailed circuit design and parts procurement specifications. This set of specifications is basic to a worst-case design.

The system specification lists such factors as weight, size, power limits, and accuracy requirements; the environments for thermal, radiation, vibration, and electromagnetic interference (EMI) are also specified. Instead of stating in the system specification minimum and maximum temperatures for the outer sides of electronic packages, the Centaur Project Office has found it desirable to specify a model for the thermal environment. From this model, a thermal analysis can predict temperature ranges for a package of a certain physical shape. These predicted minimum and maximum package temperatures with a 10° C margin added then become a part of the package specification.

A system specification that is frequently overlooked or considered uneconomical to impose is an EMI specification. System designers should consider the need for imposing an EMI specification on the contractors of electronic systems for space vehicles. The cost and weight penalty incurred to meet this requirement is justified by past experience. The Lewis Research Center has written and imposed an EMI specification (ref. 2) on its Centaur contractors. A few of the highlights of the Centaur EMI specifications are as follows:

(1) No malfunction or performance degradation shall occur when the equipment is subjected to a transient ±50-volt, 100-microsecond pulse source applied in parallel with a 28-volt power source or subjected to a 1-volt rms, 60-hertz to 15-kilohertz sine wave source applied in series with each ungrounded power line.

(2) Narrow-band conducted interference current on each input power line shall be limited to 100 milliamperes in the frequency range of 30 hertz to 3 kilohertz, decreasing to 10 microamperes at 1 megahertz.

(3) Each low-level command and signal circuit shall use a shielded twisted pair.

The imposition of a system EMI specification has an effect on lower level specifications. For example, the circuit specification for an amplifier would include the characteristic of ripple on an input dc voltage. The specification for this ripple considers the minimum attentuation of the EMI filter and power supply regulator to maximum EMI on the prime power line.

The functional specifications for each module or subsystem serve as the link between the system specifications and the individual circuit specifications. A memory module would be an example of a subsystem for a general purpose digital computer system. The functional specifications for the subsystem are derived from the system specification as the result of the system error being budgeted among the various subsystems.

The circuit specifications are derived from the functional specifications for a subsystem. A formal set of complete detailed circuit specifications allows the circuit designer to translate system requirements to flight hardware with a minimum of difficulty. Without complete specifications, the circuit designer probably will either neglect some important requirement or impose his own personal specification. This results in either (1) overdesigned circuits that are complicated and have too many critical parts or (2) inadequate circuits that will probably result in redesigns or difficult and costly manufacturing processes. A proper circuit specification must include, but is not necessarily limited to, the following:

(1) Available power supply voltages and their output characteristics, including the magnitude and frequency range of noise and ripple
(2) Noise and ripple that the circuit is allowed to inject back into the power supply lines
(3) Load variations
(4) Input-output signal characteristics
(5) Circuit transfer function
(6) Input and output impedance requirements
(7) Environmental conditions

The circuit specification should always allow for worst-case variations. The subsystem error is budgeted among the individual circuits that make up the subsystem. During the concept design phase, several iterations of selecting circuit topology together with some breadboarding and preliminary analysis may be necessary to arrive at a feasible adjustment of the subsystem error budget among the circuits.

THERMAL AND MECHANICAL DESIGN

A thorough formal thermal and mechanical design should complement the worst-case

circuit design. The need for preliminary thermal and mechanical design has already been discussed. During the detailed design phase, multinode computer thermal analysis programs are used to predict worst-case temperatures throughout the electronic package during the prelaunch and flight periods for the space vehicle. Examples of thermal concern would be the maximum junction temperature of a power transistor and the maximum thermal gradient across a memory core plane.

An important aspect to be considered in the mechanical design is the resonant vibration frequencies (and their magnitudes) of the electronic package housing and of the modules attached to the housing. The magnitude of vibration at the resonant frequencies should be low enough and separated enough in frequency so that an acceptable vibration level is experienced by the electronic parts in a circuit.

The analysis portion of the thermal and mechanical design needs to be confirmed by tests as soon as possible. Of course, design evaluation tests are performed on the prototype model of the system.

DESIGN GROUND RULES

To ensure a uniform design process, circuit designers should use a common set of design ground rules. Examples of items to be included in the design ground rules are as follows:

(1) Common derating figures for performance and stress parameters. A derating document listing amounts of derating for various classes of circuit parameters should be published.

(2) Selection of electronic parts from a preferred parts document to ensure use of established reliability parts. A procedure for qualifying needed parts that are not on the preferred parts document also should be specified. Application rules should be contained in this preferred parts document.

(3) Use of designated minimum and maximum temperatures for the initial design effort. The part case or circuit board temperatures for an individual circuit module cannot be predicted until the circuit has been designed and its location pinpointed with respect to other circuit modules. Therefore, a conservative educated guess for the minimum and maximum temperatures must be made based on a rough preliminary thermal analysis of the electronic package using the specified model for the thermal environment.

(4) Initial use of designated vibration and shock levels for the mechanical design of the circuit module. A maximum Q or amplification factor should be called out which will ensure that the circuit module will survive the vibration portion of the design proof test.

(5) Initial use of designated maximum expected radiation field to ensure that the circuit module will survive exposure to gamma, beta, and other particulate radiation

(6) Use of common semiconductor mathematical models and computer circuit analysis programs in the worst-case design process. For example, only one mathematical model of a uA709 integrated circuit operational amplifier should be used by all circuit designers.

(7) A check list of items for preparing circuit specifications, such as

(a) Gain and phase margins for circuits utilizing feedback such as regulators and operational amplifiers

(b) Output impedance against frequency for power supplies

(c) Maximum noise amplitude over a specified frequency range injected back into dc power lines from a circuit module

(d) Maximum noise over a specified frequency range that can be tolerated on a dc power line into a circuit module

(e) Propagation delays, rise times, fan-in, and fan-out for integrated digital circuits

DERATING DOCUMENT AND PREFERRED PARTS LIST

A derating document is required to ensure a uniform derating of electronic design parameters. The derating document lists all the performance and stress parameters that should be derated for each part family such as transistors. A numerical derating is also given for each parameter. As explained earlier, the derating document is used by all circuit designers in the worst-case design process. A common derating document is used by all electronic design contractors for the Centaur launch vehicle.

Performance parameters are those design parameters that affect performance and accuracy results in the worst-case design of the electronic system; an example of a performance parameter would be the current transfer ratio (beta) of a transistor that affects the gain of an amplifier. Other examples of performance parameters are listed in table I.

TABLE I. - PERFORMANCE PARAMETERS FOR WHICH DERATING MUST BE APPLIED

Transistors	Zener diodes	Fixed capacitors (paper-film dielectric)	Resistors
Current transfer ratio	Forward voltage drop	Capacitance value	Resistance value
Leakage currents	Reverse current	Ripple current	Temperature coefficient of resistance value
Saturation voltage	Temperature coefficients	Temperature coefficient of capacitance	
Gain-bandwidth product	Impedance	Leakage current	
Capacitance	Breakdown voltage	Surge current	
Offset voltage, matched pair			

Stress parameters are those design parameters that reliability engineers ordinarily use in the calculation of system reliability; an example of a stress parameter would be the emitter-to-collector voltage rating of a transistor. Other examples of stress parameters are given in table II. Performance parameters are derated to account for parameter variations during the useful lifetime of a part, and this numerical derating or tolerance is added to the initial purchase tolerance. Stress parameters are derated primarily to enhance reliability; for example, an added reliability margin is obtained by limiting the maximum allowable emitter-to-collector voltage to two-thirds of the manufacturer's specified maximum voltage.

TABLE II. - STRESS PARAMETERS FOR WHICH DERATING MUST BE APPLIED

Integrated circuits	Transistors	Capacitors
Supply voltage	Junction voltage	Voltage
Junction temperature	Device currents	-------

An example of the use of an end-of-life derating for a performance parameter follows: If a designer decides to use a paper capacitor with a value of 0.001 microfarad and a purchase tolerance of ±5 percent, he would refer to the project derating document to determine how much of an end-of-life derating tolerance must be added to the purchase tolerance. If the end-of-life derating for the capacitance value is ±10 percent, the capacitance value variation that he must allow for in the worst-case design is ±15 percent.

A simple example of derating a stress parameter would be using the two-thirds value for the derating factor of the maximum allowable emitter-to-collector voltage of a transistor. If the manufacturer rates this voltage at 60 volts, the designer would use two-thirds of 60 volts, or 40 volts for the maximum allowable voltage.

End-of-life derating values for performance parameters are conservative. In cases where these values are causing problems in worst-case design, a more realistic value may be obtained by reviewing a part derating matrix that details the various environmental factors that contribute to the derating tolerance; if justified then, certain environments or tests can be eliminated that will decrease the end-of-life derating. An example of a part derating matrix is shown in table III for a fixed solid tantalum dielectric capacitor. It can be seen that the total derating tolerance of ±8 percent is obtained by taking the root sum square of the factors that contribute to the end-of-life variation of the capacitance value. If the factors were added directly, the derating

TABLE III. - DERATING MATRIX FOR FIXED

SOLID TANTALUM DIELECTRIC CAPACITOR

	Capacity value, percent	Ripple current, percent	Temperature coefficient of capacitance	Leakage current, percent	Surge current, percent
Temperature cycling, soldering, thermal shock and moisture resistance	±3	1	0	10	5
Vibration, acceleration, and mechanical shock	±2	1	0	10	2
Atmospheric pressure and salt atmosphere	±1	0	0	5	0
Storage life	±5	2	2	100	25
Operating life	±5	2	2	400	25
Root-sum-square value	±8	3.2	2.8	413	35.8

tolerance would be ±16 percent. In this sense, the derating tolerance is not a worst-case figure; however, since the factors are conservative and are not correlated, it is a realistic approach.

The Centaur Project Office controls the usage of part types by having its contractors submit a preferred parts document and a nonstandard parts list for approval. An electronics designer is required to use a part from the preferred parts list if at all possible. If for some reason the designer wants to use a part not on the preferred parts list, a nonstandard part usage request must be submitted to NASA for review and approval. A nonstandard part usage request must be submitted for each circuit application. Considerable written justification must be contained in a nonstandard part request. NASA investigates all the technical data on a nonstandard part before it is approved for use.

WORST-CASE AND STATISTICAL CIRCUIT DESIGN PROCEDURES

A worst-case circuit design approach is desirable for space vehicle electronic systems. This approach ensures that the reliability and performance specifications of the electronic systems can be met with a minimum of difficulty. A worst-case circuit design is really an iteration of selecting a circuit topology, preparing a circuit model, performing a worst-case circuit analysis of the model, and comparing the results of the

worst-case analysis with the circuit specifications. The worst-case design is carried on in the detailed design phase of figure 1. The worst-case circuit analysis uses performance and stress parameter limit values that have been derated per the derating document. The signs of limit values used are such as to produce the least acceptable output characteristic for the circuit. If, as a result of the analysis, the circuit does not meet its specification, the circuit topology must be modified or new design limit values selected. A circuit analysis is then performed on the modified circuit topology. The cycle is repeated until the circuit specifications are met. Sometimes the circuit specification or parameter derating can be relaxed to satisfy the analysis.

Depending on the type and complexity of the circuit, either a hand or a computer-aided analysis is used. Judgement must be exercised to arrive at the optimum mix of hand and computer-aided analysis. Hand analysis has generally been used for a circuit topology of digital-type integrated circuits such as would be found in the logic section of a digital computer. Computer-aided analysis has generally been used for a circuit topology of linear-type integrated circuits and discrete components such as would be found in the input-output section of a digital computer.

There are some cases for which the circuit specifications are so tight that a true worst-case design is not practical. For these cases, with NASA approval, a statistical limit value design is used. In this statistical design process, a circuit is broken down into subblocks. For example, a regulated power supply circuit could be divided into a reference voltage block, an error amplifier block, and a series regulator block. A worst-case analysis is then performed on each circuit block using derated limit values for each circuit parameter. The worst-case analysis of each block is such that a least acceptable power supply characteristic is produced for a worst-case combination of limit values for the circuit block. Instead of adding directly the errors contributed by each circuit block, the root-sum-square value of the errors is calculated to arrive at a figure for a power supply characteristic such as phase margin. The root-sum-square method is justified if the errors are not correlated; however, it must be remembered that this is not a true worst-case design.

COMPUTER CIRCUIT ANALYSIS PROGRAMS AND SEMICONDUCTOR MODELS

The use of computer circuit analysis programs as a design tool has made the worst-case circuit design practical. The length of time required for a worst-case analysis has been reduced to a feasible level, and the analysis can be much more accurate. Previously, when hand calculations were used, simplifying assumptions had to be made in modeling the semiconductors. This reduced the accuracy of the analysis significantly for many cases. Most circuit analysis programs are written with an electronics engineer

in mind. The engineer needs no computer programming experience. The design engineer just labels the voltage nodes and current branches of the circuit model, and the input data to the computer are a simple format describing the circuit model.

In a few instances, a worst-case analysis is performed directly when both plus and minus tolerance limit values for each circuit parameter are presented in the input data to the computer. However, for most ac and transient-type analysis programs, the designer must specify the sign for the tolerance of the limit value of a parameter so as to produce a worst-case condition for a circuit.

Circuit analysis programs that have been used successfully by Centaur contractors are ECAP, NET-1 (ref. 3), and SCEPTRE (ref. 4). A contractor has also used an in-house program to determine sensitivity parameters for a worst-case analysis of ac linear circuits. Other circuit analysis programs that could be used are CIRCUS (ref. 5) and NASAP (ref. 6). ECAP is used for linear dc, ac, and transient circuit analyses. It also has the capability of nonlinear analysis by the use of piecewise linear approximations. NET-1 and SCEPTRE are used for nonlinear dc and transient circuit analyses.

A circuit analysis computer program cannot predict performance accurately unless the mathematical models for semiconductors represent closely the characteristics of the actual physical devices used in the final design. In fact, the most difficult job in designing a circuit with the aid of circuit analysis computer programs is obtaining the values of the parameters for the semiconductor models.

By combining resistors, capacitors, and voltage and current sources in a circuit topology, semiconductors can be modeled for inclusion into a circuit to be analyzed. Not only have discrete diodes and transistors been modeled, but also mathematical models have been developed for monolithic integrated linear circuits.

The mathematical model used to represent an integrated-circuit operational amplifier is a black box equivalent circuit that, under nominal (or measured) conditions, very accurately duplicates the characteristics of the actual integrated circuit, usually with feedback and forward compensation elements included. All the integrated circuit parameters that are important to feedback stability analysis are incorporated into the model. The designer may vary all model parameters (including external feedback elements) so as to obtain worst-case conditions. Worst-case (derated) limits are established for each of the model parameters by the use of vendor specifications, application notes, direct vendor contract, measured values, and Centaur derating procedures. No attempt is made to simulate each transistor stage within the integrated-circuit wafer. Operational amplifiers that have been modeled by Centaur contractors include the uA709, CA3015, uA741, and LM101. Figure 2 is the schematic diagram of the uA709 model as used for ac analysis on ECAP. This schematic diagram is included only to illustrate the complexity of the model.

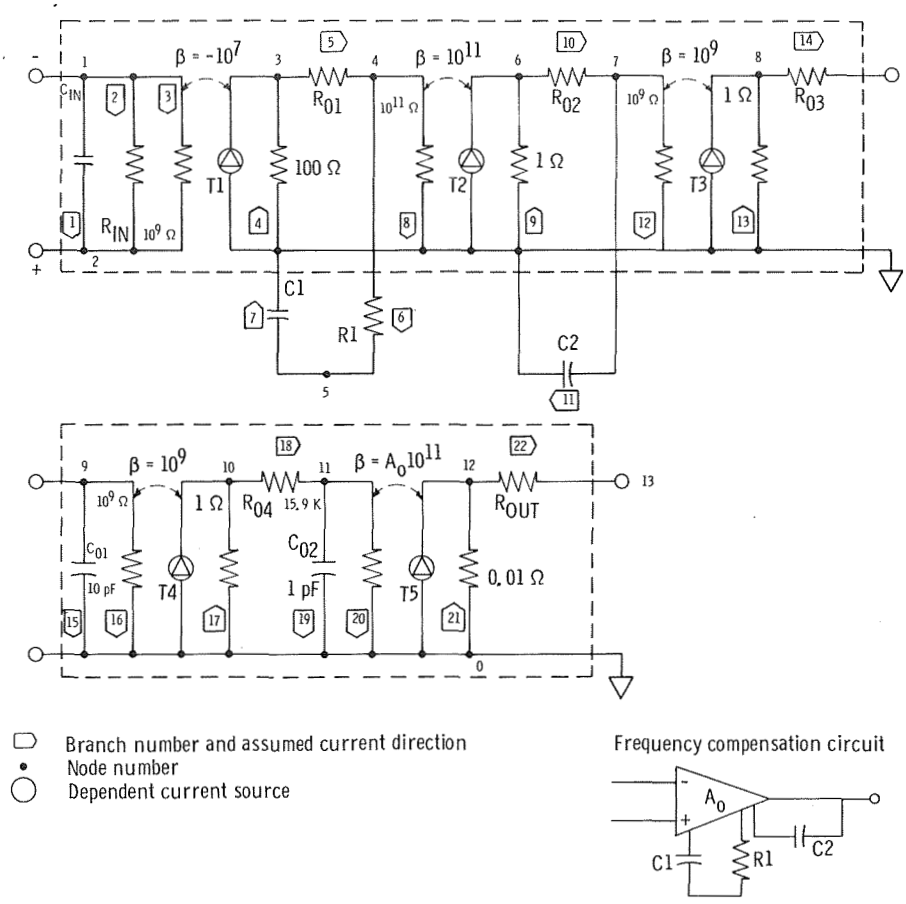

Figure 2. - μA709 ECAP ac equivalent circuit model.

DESIGN REVIEWS

An important control used in the worst-case design process is the design review between customer and contractor. Design reviews allow customers such as NASA to keep in close touch with the design of the electronic system as it progresses from the specification stage to the production stage.

As shown in the design block diagram of figure 1, a concept design review is held shortly after the functional specifications have been agreed upon and the contractor has gone through the concept design stage. The purpose of the concept review is to select a design mechanization based on the work done in the concept design stage. Also, the design approach is considered for the selected design mechanization. Design approach considers such items as the type of analysis to be performed (transient, small-signal ac) and the type of computer program to be used in the analysis portion of the design cycle.

Progress reviews are held as needed between the concept and final design reviews. The purpose of these reviews is to consider design problem areas, interface changes

with other vehicle systems, and use of nonstandard parts. The purpose of the final design review is to compare analytical and test results with the specifications. If results are favorable, formal approval is given to proceed to the prototype construction stage.

The NASA project office is represented by a team of specialists at these design reviews. They include a circuit analyst, an electronic part specialist, a reliability and/or quality control specialist, and a system engineer. A week or two prior to the review, an agenda and a technical data pack are sent by the contractor for the NASA technical team to study. The specialist is expected to review the data in his area and to prepare a list of comments and questions for the design review presentation. Between reviews, the technical team does independent analysis, fact finding, and part evaluation to provide a technical data basis for future design reviews.

At the design review, customer and contractor review the design to ensure that specifications have been met and that the design approach agreed upon has been followed. The results of the design review are documented, and the contractor may be required to make some changes in the specifications or design.

CONCLUDING REMARKS

Use of the described technical management procedures results in an electronic system capable of meeting its performance and reliability specifications with a minimum of difficulty. The technical management procedure consists of applying controls for a worst-case design in a rigorous systematic manner. The following specific controls are used:

(1) Complete hierarchy of specifications
(2) Thermal and mechanical design to meet worst-case conditions
(3) Design ground rules
(4) Derating document and preferred parts list
(5) Worst-case circuit design procedures
(6) Computer circuit analysis programs
(7) Design reviews

These technical management procedures are being used successfully by the NASA Lewis Research Center in the design and development of launch vehicle systems.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, May 22, 1970,
491-02.

REFERENCES

1. Anon.: 1620 Electronic Circuit Analysis Program (ECAP) (1620-EE-02X) User's Manual. IBM Application Program File H20-0170-1, 1965.

2. Anon.: Specification for Electromagnetic Interference Control Environmental Requirements and Test Procedures for the Centaur Launch Vehicle, CS-EMC-1A, NASA Lewis Research Center, Centaur Project Office, Aug. 1967.

3. Malmberg, Allan F.; Cornwell, Fred L.; and Hofer, Florian N.: NET-1 Network Analysis Program: 7090/94 Version. Rep. LA-3119, Los Alamos Scientific Lab., Aug. 10, 1964.

4. Mathers, H. W.; Sedore, S. R.; and Sents, J. R.: Automated Digital Computer Program for Determining Responses of Electronic Circuits to Transient Nuclear Radiation (SCEPTRE). Vol. I. IBM Space Guidance Center, Owego, N.Y., IBM File 66-928-611, Feb. 1967.

5. Milliman, L. D.; Massena, W. A.; and Dickhant, R. H.: CIRCUS - A Digital Computer Program for Transient Analysis of Electronic Circuits - User's Guide. Rep. AD-346-1, Boeing Co. and Harry Diamond Labs., Jan. 1967.

6. Bach, R. E., Jr.; and Olendzenski, P. A.: NASAP for On-Line Applications. Vol. 1. A User's Guide. Elect. Eng. Dept., Northeastern Univ., Jan. 1969. (Work done under Contract NAS12-2036.)

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